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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,804	09/09/2003	Sayeed Ahmed	130209.508	1805

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SIEMENS CORPORATION
INTELLECTUAL PROPERTY DEPARTMENT
170 WOOD AVENUE SOUTH
ISELIN, NJ 08830

EXAMINER	
LAXTON, GARY L	

ART UNIT	PAPER NUMBER
2838	

MAIL DATE	DELIVERY MODE
05/01/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/658,804	AHMED ET AL.	
	Examiner	Art Unit	
	Gary L. Laxton	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,11-14 and 20-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,11-14 and 20-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Reopening of Prosecution

1. In view of the appeal brief filed on 1/30/2008, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

/Akm Enayet Ullah/

Supervisory Patent Examiner, Art Unit 2838

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-3 and 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parkhill et al. in view of Lindemann et al. (US 6,507,108)

Parkhill et al. disclose a power module (e.g. fig 2), comprising: a module housing; integrate cold plate (e.g. header 27 & base plate 61); a set of DC terminals (21, 23) accessible from an exterior of the module; a DC bus (25) electrically coupled to the pair of input terminals; at least three pairs of AC terminals (15, 17, 19) accessible from the exterior of the module housing; and an inverter circuit (e.g. figs. 3, 9 and 10) contained within the module housing, the inverter circuit configurable to selectively switch between at least three output states (positive voltage, negative voltage and zero voltage. i.e. in order to produce a sine wave output for AC loads) and electrically coupled between the set of DC terminals and at least one of the pairs of AC terminals.

However, Parkhill et al. do not disclose wherein the cold plate includes a direct copper bonded substrate attached to a base plate by a solder layer.

Lindemann et al. teach that integrated cold plate are nothing new in the art. Lindemann et al. also teach that direct copper bonded substrate is nothing new in the art. In fact, direct copper bonded substrate attached to a base plate by solder is standard operating procedure in the art and

it is most certainly nothing novel in the art. That is, Lindemann et al. expressly teach that when manufacturing power semiconductor modules, it is generally necessary to electrically insulate the power semiconductors or power semiconductor chips from the base body or heat sink which is used to dissipate heat. Ceramic isolators in disk form and with a metallized surface are widely used for this purpose. For example, direct copper bonding (DCB) substrates are used on one of whose surfaces the power semiconductor chips are essentially arranged, while the other surface is thermally coupled to the heat sink. With regard to thermal coupling to the cooling medium--typically via the underneath of the component--that surface of the DCB ceramic to which the chips are not fitted forms the underneath of the component in a module which has a DCB bottom. As a rule, thermal coupling is achieved by pressing onto a typically metallic heatsink, from which heat is extracted by a cooling medium, such as air or cooling liquid, with the boundary surface between the DCB bottom and the heat sink advantageously having to be provided with an intermediate layer composed of a thermally linking medium, for example thermally conductive paste. In a module having a bottom plate, that surface of the DCB ceramic to which the chips are not fitted is thermally coupled to a bottom plate which is generally composed of a metal or composite material; the coupling can be achieved, typically, once again using a thermally linking medium, for example thermally conductive paste, by solder or by other integral material joints, the latter in particular in the case of bottom plates composed of composite materials (col. 1 lines 10-65).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Parkhill et al. to include a cold plate that includes a direct

copper bonded substrate attached to a base plate by a solder layer as taught by Lindemann et al. to be old and well known in the art in order to cool the power converter.

5. Claims 20-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parkhill et al. and Lindemann et al. in view of Romero et al. (US 5,544,412).

Claims 20, 21, 23, Parkhill et al. and Lindemann et al. disclose the claimed subject matter in regards to claims 1 and 11 supra, except for the direct copper bonded substrate includes a first copper layer, a ceramic layer and a second copper layer fused together; or, whether the second copper layer is etched to form electrically isolated structures for selectively mounting circuit components.

Romero et al. teach that direct copper bonded substrate includes a first copper layer (e.g. 50), a ceramic layer (e.g. dielectric material 51 & 76) and a second copper layer (52) all fused together (col. 5 lines 25-35 & col. 6 lines 50-60). Moreover, Romero et al. illustrate that the second copper layer is etched to form electrically isolated structures for selectively mounting circuit components.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Parkhill et al. and Lindemann et al. to include direct copper bonded substrate includes a first copper layer, a ceramic layer and a second copper layer fused together as is the well known technique for direct bonded copper as taught by Romero et al. and to etch the second layer of copper in order mount circuit components as taught by Romero et al.

Claims 22 and 25; Parkhill et al. teach the base plate includes a first side to which the solder layer would be attached and a second side that is in thermal contact with a fluid channel for cooling the circuit components that would be mounted to the direct copper bonded substrate.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US 6,166,937 Yamamura et al. disclose mounting semiconductor components (4) to a heat sink/cold plate (1) including a solder layer (5); US 5,574,312 Bayerer et al. disclose substrates are soldered to heat sinks by DCB aluminum oxide ceramic on copper.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary L. Laxton whose telephone number is (571) 272-2079. The examiner can normally be reached on Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Akm Ullah can be reached on (571) 272-2361. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

4/25/2008

/Gary L. Laxton/
Primary Examiner
Art Unit 2838

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

/Akm Enayet Ullah/

Supervisory Patent Examiner, Art Unit 2838